CLAIMS

1. A differential multi-PAM extractor circuit comprising:

an upper LSB sampler circuit configured to receive a differential multi-PAM input signal and a first differential reference signal, and to generate a first differential sampled output signal;

a lower LSB sampler circuit configured to receive the differential multi-PAM input signal and a second differential reference signal, and to generate a second differential sampled output signal; and

a combiner circuit configured to receive the first differential sampled output signal and the second differential sampled output signal, and to generate a differential LSB output signal indicating an LSB value of the differential multi-PAM input signal.

2. The differential multi-PAM extractor circuit of claim 1, further comprising:

an MSB sampler circuit configured to receive the differential multi-PAM input signal and a reference signal, and to generate a differential MSB output signal indicating an MSB value of the differential multi-PAM input signal.

3. The differential multi-PAM extractor circuit of claim 1, wherein the first differential reference signal and the second differential reference signal are the same differential reference signal.

4. The differential multi-PAM extractor circuit of claim 1, wherein the first differential reference signal and the second differential reference signal are different differential reference signals.

5. The differential multi-PAM extractor circuit of claim 1, wherein the upper LSB sampler circuit and the lower LSB sampler circuit comprise:

first and second pairs of input transistors configured to receive the differential multi-PAM input signal;

first and second pairs of offset transistors, coupled to the first and second pairs of input transistors, respectively, and configured to receive the first and second differential reference signals, respectively;

first and second linear loads coupled to the first and second pairs of input transistors and the first and second pairs of offset transistors, respectively; and

a plurality of current sources coupled to the first and

second pairs of input transistors and the first and second pairs of offset transistors;

wherein first and second differential output signals are generated based upon the values of the differential multi-PAM input signal and the first and second differential reference signals, respectively.

6. The differential multi-PAM extractor circuit of claim 5, wherein the upper LSB sampler circuit and the lower LSB sampler circuit further comprise:

first and second sampler devices, coupled to the first and second pairs of input transistors and the first and second pairs of offset transistors, respectively, and configured to sample the first and second differential output signals, respectively, and to generate the first and second differential sampled output signals, respectively.

7. The differential multi-PAM extractor circuit of claim 6, wherein the combiner circuit comprises:

an exclusive OR logic device configured to receive the first and second differential sampled output signals and to generate the differential LSB output signal.

8. The differential multi-PAM extractor circuit of claim 6, wherein the first and second sampler devices are clocked at a sampling rate.

9. The differential multi-PAM extractor circuit of claim 5, wherein the first and second differential reference signals have similar voltage levels, but are opposite in polarity.

10. The differential multi-PAM extractor circuit of claim 5, wherein the first and second differential reference signals have a common-mode similar to the differential multi-PAM input signal.

11. The differential multi-PAM extractor circuit of claim 1, wherein the upper LSB sampler circuit and the lower LSB sampler circuit comprise:

first and second pairs of input transistors configured to receive the differential multi-PAM input signal;

first and second pairs of offset transistors, coupled to the first and second pairs of input transistors, respectively, and configured to receive the first and second differential reference signals, respectively;

first and second nonlinear loads coupled to the first and

second pairs of input transistors and the first and second pairs of offset transistors, respectively; and

a plurality of switches coupled to the first and second pairs of input transistors and the first and second pairs of offset transistors;

wherein first and second differential output signals are generated based upon the values of the differential multi-PAM input signal and the first and second differential reference signals, respectively.

12. The differential multi-PAM extractor circuit of claim 11, wherein the plurality of switches are clocked at a sampling rate.

13. The differential multi-PAM extractor circuit of claim 12, wherein the first and second nonlinear loads are clocked at the sampling rate for sampling the first and second differential output signals, respectively, and for generating first and second differential sampled output signals, respectively.

14. The differential multi-PAM extractor circuit of claim 13, wherein the combiner circuit comprises:

an exclusive OR logic device configured to receive the

first and second differential sampled output signals and to generate the differential LSB output signal.

15. The differential multi-PAM extractor circuit of claim 11, wherein the first and second differential reference signals have similar voltage levels, but are opposite in polarity.

16. The differential multi-PAM extractor circuit of claim 11, wherein the first and second differential reference signals have a common-mode similar to the differential multi-PAM input signal.

17. A differential multi-PAM extractor circuit comprising:

a pair of input transistors configured to receive a differential multi-PAM input signal;

a pair of equalization transistors, coupled to the pair of input transistors, and configured to receive a differential equalization signal;

a linear load coupled to the pair of input transistors and the pair of equalization transistors; and

a pair of current sources coupled to the pair of input transistors and the pair of equalization transistors.

18. The differential multi-PAM extractor circuit of claim 17, wherein the differential offset signal has a common-mode similar to the differential multi-PAM input signal.

19. A differential multi-PAM extractor circuit comprising:

a pair of input transistors configured to receive a differential multi-PAM input signal;

a pair of equalization transistors, coupled to the pair of input transistors, and configured to receive a differential equalization signal;

a nonlinear load coupled to the pair of input transistors and the pair of equalization transistors; and

a pair of switches coupled to the pair of input transistors and the pair of equalization transistors.

20. The differential multi-PAM extractor circuit of claim 19, wherein the pair of switches are clocked at a sampling rate.

21. The differential multi-PAM extractor circuit of claim 20, wherein the nonlinear load is clocked at the sampling rate for sampling a differential output signal, and for generating a sampled output signal.

22. The differential multi-PAM extractor circuit of claim 19, wherein the differential equalization signal has a common-mode similar to the differential multi-PAM input signal.

23. A differential multi-PAM extractor circuit comprising:

first and second pairs of input transistors configured to receive a differential multi-PAM input signal;

first and second pairs of adjustable resistive elements, coupled to the first and second pairs of input transistors, respectively, and configured to receive a differential control signal;

a load coupled to the first and second pairs of input transistors; and

a pair of current sources coupled to the first and second pairs of adjustable resistive elements, respectively.

24. The differential multi-PAM extractor circuit of claim 23, wherein the differential control signal is applied to the first and second pairs of adjustable resistance elements so as to adjust their resistance value.

25. The differential multi-PAM extractor circuit of claim 24, wherein the first and second pairs of adjustable resistance

elements comprise field effect transistors having gates that are controlled by the differential control signal.

26. A differential multi-PAM extractor circuit comprising:

first and second pairs of adjustable voltage sources connected in series with signal paths for a differential multi-PAM input signal, the first and second pairs of adjustable voltage sources configured to receive a differential control signal;

first and second pairs of input transistors, coupled to the first and second pairs of adjustable voltage sources, respectively, and configured to receive voltage adjusted differential multi-PAM input signals from the first and second pairs of adjustable voltage sources, respectively;

a load coupled to the plurality of pairs of unbalanced input transistors; and

a pair of current sources coupled to the first and second pairs of input transistors, respectively.

27. The differential multi-PAM extractor circuit of claim 26, wherein the differential control signal is applied to the first and second pairs of adjustable voltage sources so as to adjust their voltage value.

28. The differential multi-PAM extractor circuit of claim 26, wherein the first and second pairs of adjustable voltage sources comprise resistor divider circuits.

29. The differential multi-PAM extractor circuit of claim 28, wherein the resistor divider circuits comprise an adjustable resistive element.

30. The differential multi-PAM extractor circuit of claim 28, wherein the resistor divider circuits comprise an adjustable voltage source.

31. A differential multi-PAM extractor circuit comprising:

a differential amplifier circuit configured to receive a differential multi-PAM input signal and to generate an amplified differential multi-PAM signal;

a differential automatic gain control circuit, coupled to the differential amplifier circuit, and configured to control gain in the differential amplifier circuit;

a first differential sampler circuit, coupled to the differential amplifier circuit and the differential automatic gain control circuit, and configured to sample the amplified

differential multi-PAM signal and to generate a first output signal indicating a most significant bit value of the differential multi-PAM input signal; and

a second differential sampler circuit, coupled to the differential amplifier circuit and the differential automatic gain control circuit, and configured to sample the amplified differential multi-PAM signal and to generate a second output signal indicating a least significant bit value of the differential multi-PAM input signal.

32. The differential multi-PAM extractor circuit of claim 31, wherein the first and second differential sampler circuits are clocked at a sampling rate.

33. A differential multi-PAM extractor circuit comprising:

a first differential amplifier circuit configured to receive a differential multi-PAM input signal and to generate a first amplified differential multi-PAM signal;

a second differential amplifier circuit configured to receive the differential multi-PAM input signal and to generate a second amplified differential multi-PAM signal;

a first differential automatic gain control circuit, coupled to the first differential amplifier circuit, and

configured to control gain in the first differential amplifier circuit;

a second differential automatic gain control circuit, coupled to the second differential amplifier circuit, and configured to control gain in the second differential amplifier circuit;

a first differential sampler circuit, coupled to the first differential amplifier circuit and the first differential automatic gain control circuit, and configured to sample the first amplified differential multi-PAM signal and to generate a first output signal indicating a most significant bit value of the differential multi-PAM input signal; and

a second differential sampler circuit, coupled to the second differential amplifier circuit and the second differential automatic gain control circuit, and configured to sample the second amplified differential multi-PAM signal and to generate a second output signal indicating a least significant bit value of the differential multi-PAM input signal.

34. The differential multi-PAM extractor circuit of claim 33, wherein the first and second differential sampler circuits are clocked at a sampling rate.

35. A differential multi-PAM extractor circuit comprising:

a first differential amplifier circuit configured to receive a differential multi-PAM input signal and to generate a first amplified differential multi-PAM signal;

a second differential amplifier circuit configured to receive the differential multi-PAM input signal and to generate a second amplified differential multi-PAM signal;

a differential automatic gain control circuit, coupled to the first differential amplifier circuit and the second differential amplifier circuit, and configured to control gain in the first differential amplifier circuit and the second differential amplifier circuit based at least in part upon the first amplified differential multi-PAM signal;

a first differential sampler circuit, coupled to the first differential amplifier circuit and the differential automatic gain control circuit, and configured to sample the first amplified differential multi-PAM signal and to generate a first output signal indicating a most significant bit value of the differential multi-PAM input signal; and

a second differential sampler circuit, coupled to the second differential amplifier circuit, and configured to sample the second amplified differential multi-PAM signal and to generate a second output signal indicating a least significant

bit value of the differential multi-PAM input signal.

36. The differential multi-PAM extractor circuit of claim 35, wherein the first and second differential sampler circuits are clocked at a sampling rate.

37. A differential multi-PAM extractor circuit comprising:

a plurality of differential amplifier circuits configured to receive a differential multi-PAM input signal and to generate a plurality of amplified differential multi-PAM signals;

a plurality of adjustable offset voltage sources, coupled to the plurality of differential amplifier circuits, respectively, and configured to provide a plurality of offset voltage signals to the plurality of differential amplifier circuits, respectively; and

a plurality of differential multiple-sampler circuits, coupled to the plurality of differential amplifier circuits, respectively, and configured to multiple-sample the plurality of amplified differential multi-PAM signals, respectively, to generate a plurality of multiple-sampled multi-PAM signals, respectively, and to determine a most significant bit value and a least significant bit value of the differential multi-PAM input signal.

38. The differential multi-PAM extractor circuit of claim 37, further comprising:

a plurality of deserializer circuits, coupled to the plurality of differential multiple-sampler circuits, and configured to receive the plurality of multiple-sampled multi-PAM signals and to generate parallel data blocks for determining the most significant bit value and the least significant bit value of the differential multi-PAM input signal.

39. The differential multi-PAM extractor circuit of claim 38, wherein the plurality of deserializer circuits also generate parallel data blocks for clock data recovery purposes.

40. The differential multi-PAM extractor circuit of claim 38, wherein the plurality of deserializer circuits also generate parallel data blocks for calibration of the plurality of differential multiple-sampler circuits.

41. The differential multi-PAM extractor circuit of claim 38, further comprising:

a parallel digital multiplexer, coupled to the plurality of deserializer circuits, and configured to direct the parallel

data blocks.

42. The differential multi-PAM extractor circuit of claim 38, wherein the plurality of deserializer circuits are clocked at a sampling rate.

43. The differential multi-PAM extractor circuit of claim 42, wherein the plurality of differential multiple-sampler circuits are clocked at a sampling rate.

44. The differential multi-PAM extractor circuit of claim 43, further comprising:

clock generation circuitry configured to generate clock signals for the plurality of differential multiple-sampler circuits and the plurality of deserializer circuits.

45. The differential multi-PAM extractor circuit of claim 37, further comprising:

a plurality of analog multiplexers, mostly coupled to the plurality of differential amplifier circuits, and configured to direct the plurality of amplified differential multi-PAM signals and a differential multi-PAM calibration reference signal to the plurality of differential multiple-sampler circuits.

46. The differential multi-PAM extractor circuit of claim 45, further comprising:

a state machine configured to control the states of the plurality of analog multiplexers.

47. The differential multi-PAM extractor circuit of claim 45, wherein each of the plurality of differential multiple-sampler circuits comprises:

an adjustable current source;

a plurality of charge storage devices, switchably coupled to the adjustable current source, and configured to store a plurality of charges, respectively, supplied by the adjustable current source; and

a plurality of clocked sampler devices, coupled to the plurality of analog multiplexers and the plurality of charge storage devices, respectively, and configured to periodically receive the differential multi-PAM calibration reference signal for calibrating a respective stored charge.

48. The differential multi-PAM extractor circuit of claim 47, wherein each of the plurality of differential multiple-sampler circuits further comprises:

a plurality of switching devices, coupled between the adjustable current source and the plurality of charge storage devices, respectively, and configured to periodically connect the adjustable current source to the plurality of charge storage devices.

49. The differential multi-PAM extractor circuit of claim 48, further comprising:

a state machine configured to control the states of the plurality of switching devices.

50. The differential multi-PAM extractor circuit of claim 47, wherein each of the plurality of differential multiple-sampler circuits further comprises:

an analog multiplexing device, coupled between the adjustable current source and the plurality of charge storage devices, and configured to periodically connect the adjustable current source to the plurality of charge storage devices.

51. The differential multi-PAM extractor circuit of claim 50, further comprising:

a state machine configured to control the state of the analog multiplexing device.

52. The differential multi-PAM extractor circuit of claim 47, wherein each of the plurality of differential multiple-sampler circuits further comprises:

a controller configured to control the adjustable current source.

53. The differential multi-PAM extractor circuit of claim 52, wherein the controller is a state machine.

54. The differential multi-PAM extractor circuit of claim 37, further comprising:

a state machine configured to control the states of the plurality of differential multiple-sampler circuits.

55. The differential multi-PAM extractor circuit of claim 37, wherein at least one of the plurality of adjustable offset voltage sources comprises a precision digital-to-analog converter.